UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,379	10/15/2003	Takashi Kobayashi	500.39879VX1	8866

20457 7590 10/20/2005

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/684,379	KOBAYASHI, TAKASHI	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *34-36 and 40-42* is/are allowed.

6)☒ Claim(s) *37 and 39* is/are rejected.

7)☒ Claim(s) *38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/811,444.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *15 October 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 37 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crivelli et al. (USPN 6,319,780 B2) in view of Krivokapic et al. (USPN 6,396,108 B1).

3. In reference to claim 37, Crivelli et al. (USPN 6,319,780 B2, hereinafter referred to as the "Crivelli" reference) discloses a fabrication method which meets the claim. Figures 1-8 of Crivelli illustrates a process for producing a nonvolatile semiconductor memory device with a plurality of memory cells each having a floating gate (13a) formed on a semiconductor substrate with the interposition of a tunnel dielectric film (12) and a control gate (17a) formed on the floating gate (13a) with the interposition of an interpoly dielectric film (15) and a plurality of field effect transistors each having a gate electrodes (17b or 17c) formed on the semiconductor substrate with the interposition of a gate insulating film (15 or 16). A shallow groove isolation region (11) is formed on the semiconductor substrate. A tunnel dielectric film (12) is formed on the semiconductor substrate surface in the memory cell region by a thermal oxidation method (column 3, lines 29-34). A first polycrystalline Si film (13) is deposited which becomes the floating

gate (13a). The first polycrystalline film (13) is removed in the field effect transistor formed region (figure 5). A first silicon oxide film (15) is formed on the semiconductor substrate surface which becomes a first portion of the gate insulating film (15). A second silicon oxide film (16) is deposited which becomes the interpoly dielectric film (15) and a second portion of the gate insulating film (15). A second polycrystalline Si film (17) is deposited which becomes the control gate (17a) and the gate electrodes (17b). Crivelli does not disclose the use of thermal oxidation to form the first silicon oxide film (15). However the use of thermal oxidation to form gate insulating films is well known in the art. Krivokapic et al. (USPN 6,396,108 B1, hereinafter referred to as the "Krivokapic" reference) discloses that thermal oxidation provides better gate oxides than deposited oxide processes (column 3, lines 65-67 and column 4, line 1). In view of Krivokapic, it would therefore be obvious to use thermal oxidation to form a better gate insulating film.

4. With regard to claim 39, Crivelli discloses doping the gate structures (13a, 17c) with an n-type impurity (column 3, lines 29-34 and column 4, lines 14-18) but does not disclose the use of phosphorus. However the applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416. Therefore claim 39 is not patentable over the Crivelli and Krivokapic references.

Allowable Subject Matter

5. Claims 34-36 and 40-42 are allowed.

6. Claim 38 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a fabrication process for a nonvolatile semiconductor memory device having a floating gate and a field effect transistor such that a first silicon oxide film which is formed as a portion of the gate dielectric for the field effect transistor is also formed over the nonvolatile semiconductor memory transistor portion of the device but is removed while a second silicon oxide film is deposited to form both an intergate dielectric and a second portion of the gate dielectric for the field effect transistor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800